

## REMARKS

Claims 1 - 20 remain active in this application.  
No new matter has been introduced into the application.

Claims 1 - 4, 7 - 12 and 14 - 20 (including all independent claims in the application) have been rejected under 35 U.S.C. §102 as being anticipated by Hummler. Claims 5 and 6 have been rejected under 35 U.S.C. §103 as being unpatentable over Hummler. Claim 13 has been rejected under 35 U.S.C. §103 as being unpatentable over Hummler in view of Gustafson et al. All of these grounds of rejection are respectfully traversed for the reasons of record and the further remarks presented below. Again, it is respectfully brought to the Examiner's attention that Hummler is incorporated by reference in the present application as disclosing an exemplary basic top oxide early (TOE) process over which the present invention provides significant improvements which increase processing yield and process simplifications and some of which are also applicable to top oxide nitride (TON) and top oxide late (TOL) processes, as are pointed out in the specification as originally filed and which the Examiner has, improperly, not directly addressed.

The invention is basically directed to refinements in planarization techniques which reduce artifacts such as scratching, dishing and contamination which may occur through chemical-mechanical polishing (CMP), particularly where large areas containing differentiated structures are presented when CMP is to be performed and which are not taught or suggested by Hummler.

In regard to independent claim 1, for example, amendatory language was presented in the step of "reducing height of *structures* in said first and second areas" to recite the purpose and effect of the claimed

height reduction of *structures*; specifically, "to control *step height* in said *first and second areas*". This recitation as originally filed and as later amended is directed to deglazing to recess the isolation structures IT provided in *both* the array and support areas of the chip such that *step height* is similar in both areas even though the topology may differ markedly between the array and support areas as illustrated at 58 of Figure 5 (whereas, if the isolation structures IT had not been reduced in height, a substantial step would be presented at least in the region above the isolation structure at the boundary of the array and support areas. As disclosed in paragraph [0026] reducing height of structures in both the array and support areas permits setting of isolation structure heights independently of the array top oxide application and facilitates planarization by reducing the amount of material to be removed, tending to reduce CMP artifacts. In the present action, the Examiner explicitly accords no weight to this recitation and specifically relies on processes of Hummler which do not answer the amendatory recitation or *the original recitation* of this step in claim 1.

Specifically, the Examiner relies on *separate steps* in Hummler in regard to 46 of Figures 7A which become sidewall 48 in Figure 8 in the array area 16 of Hummler and on the recessing of isolation trench 38 in the support area of Figure 1A of Hummler while explicitly asserting, without identifying any authority to do so, that "the recited purpose does not limit the scope of the claim since it does not require any additional non-recited steps". In regard to the former structures relied upon by the Examiner, it is respectfully submitted that the etching depicted in Figures 7A and 8 is for the purpose of *forming a sidewall* in a recess from a blanket

layer of material and is thus does not answer a recitation of reducing a *height* of a structure in an area of the chip; which (existing) structure has already been recited in the preamble of the claim. In regard to the recessing of isolation structure 38 at location 39 it is respectfully submitted that such isolation structures and the recessing thereof (which is disclosed to be optional) are *only* disclosed in regard to support area 18 and, moreover, the height thereof is disclosed to be critical (regardless of step height) in the support area at column 4, lines 11 - 24, of Hummler and, in fact, the following paragraph of Hummler indicates that Hummler is directed to protecting the isolation trench height so achieved during processing of the array area. Hummler certainly does not disclose or even contemplate any meritorious effect to be achieved from recessing isolation structures or any other structures in *both* the array and support areas of the chip and particularly no meritorious effects to be derived from controlling step height in *both* areas.

Therefore, it is respectfully submitted that the Examiner has not demonstrated disclosure in Hummler of reducing height of structures in *both* the array and support areas of a chip, much less in a single process and clearly not for the purpose of controlling step height in both areas; to which recitation, it is respectfully submitted to be improper for the Examiner to have accorded no weight or capacity to distinguish from Hummler. Therefore, it is respectfully submitted that Hummler does not, in fact, and cannot properly be considered to anticipate claim 1 or any of claims 2 - 11 depending therefrom.

Additionally, as pointed out in the first full paragraph of page 14 of the response filed January 10, 2007, Hummler does not teach using a polysilicon block

out mask *comprising two layers of different materials*. The present statement of the rejection is entirely silent as to this feature of the invention as recited in claim 1. While the passage relied upon by the Examiner discloses "alternative" materials for mask 44 it does not disclose a mask of two layers which are of different materials. Providing such a layered mask supports the meritorious functions of further reducing step height (and thus enhancing the effect provided by reducing height of structures in both the array and support areas as discussed above) but also provides enhanced protection as disclosed paragraph [0027] of the application. Therefore, it is respectfully submitted that the Examiner has failed to demonstrate anticipation of this feature of the claimed invention as recited in claim 1, as well.

In regard to independent claims 12 and 16, it was previously pointed out that layer 50 of Hummler, relied upon by the Examiner is, in fact, the array top oxide and that the mention of using ARC followed by a reactive ion etch (RIE) in Hummler at column 7, lines 3 - 17, is disclosed in Hummler to be simply for the purpose of opening the tops of the gate electrode contacts 34 and no planarizing effect is attributed thereto in Hummler. While planarizing by CMP is mentioned in Hummler as an alternative process for opening such contacts, it should be noted that a reactive ion etch is not necessarily sufficiently non-selective for planarization from a planar surface, as claimed, as an alternative to planarization by CMP absent the particular conditions for non-selectivity disclosed in paragraph [0036] of the present specification. In this regard, it is respectfully submitted that there is no need for (and thus no implication of planarizing by non-selective RIE) in Hummler since only the ATO and a thin layer of the

support nitride liner 42 overlying pad nitride 14 is etched while opening the gate electrode contacts. In other words and simply put, while a CMP planarizing process may be used to open contacts, an alternative process for opening contacts by RIE from a planar surface does not imply that a planar surface will be produced, as the Examiner appears to assume through hindsight, or that conditions necessary to produce a planar surface in the same process were known prior to the present invention. Thus, Hummler does not anticipate any on claims 12 - 20.

Accordingly, it is respectfully submitted that the teachings and/or suggestions contained Hummler do not support a conclusion of either anticipation or obviousness (e.g. in regard to claims 5 and 6) based on Hummler alone. Hummler clearly does not anticipate any claim as discussed above and does not provide evidence of a level of ordinary skill in the art which would support a conclusion of obviousness since it does not lead to an expectation of success in providing increased manufacturing yield through control of step height augmented in combination with use of a two layer block-out mask or planarization by non-selective etching from a planar surface. Therefore, it is respectfully submitted that grounds of rejection based on Hummler are in error and untenable and upon reconsideration, should be withdrawn. In regard to claim 13, which has been rejected based on Hummler and Gustafson et al. (which is added for teaching etching with end point detection, admittedly absent from the teachings of suggestions of Hummler), it is respectfully submitted that Gustafson et al. does not mitigate any of the deficiencies of Hummler and the Examiner has not asserted that it does; thereby also failing to make a *prima facie* demonstration of obviousness of claim 13. Further, it was previously

pointed out that use of end point detection in Hummler would defeat an asserted advantage of the process of Hummler and is thus an improper suggested modification thereof under the precedent of *In re Gordon*, 221 USPQ 1125 (Fed. Circ., 1984). Accordingly, it is respectfully submitted that the rejection of claim 13 is also improper and untenable and, upon reconsideration, should be withdrawn.

Since all rejections, objections and requirements contained in the outstanding official action have been fully answered and shown to be in error and/or inapplicable to the present claims, it is respectfully submitted that reconsideration is now in order under the provisions of 37 C.F.R. §1.111(b) and such reconsideration is respectfully requested. Upon reconsideration, it is also respectfully submitted that this application is in condition for allowance and such action is therefore respectfully requested.

If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to IBM Deposit Account No. 09-0458.

Respectfully submitted,



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